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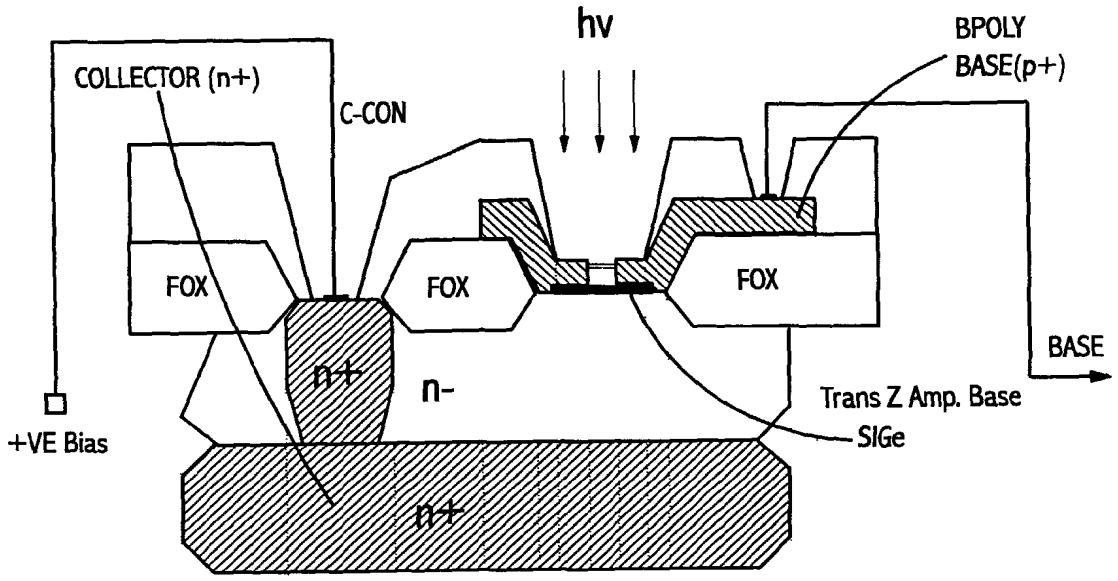
(54) Title: OPTOELECTRONIC DETECTOR AND RELATED CIRCUIT



(57) Abstract: The invention provides for a photo receiver comprising a *p-i-n* photodiode formed of a reversed biased base-collector junction of a silicon based integrated HBT device and a monolithic semiconductor structure comprising a *p-i-n* photodiode formed of a reversed bias base-collector junction of an integrated HBT device and a transimpedence amplifier arranged to be driven by an output from the HBT device, the transimpedence amplifier including a negative feedback buffer.

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Optoelectronic Detector and Related Circuit

The present invention relates to an optoelectronic detector and related circuit arrangement.

Optoelectronic detector circuits are widely used in modern high-speed Internet packet switching systems. Increasing demands on Internet package switches result in the need for high density, high speed, photo receiver arrays. One potential barrier to achieving higher packing densities is the choice of detector device, with many designs relying on the use of externally connected PIN diodes or APD's.

Conventional photo receivers compatible with monolithic integration with CMOS digital logic offer data rates of only a few Mbit/s. This is because a p-n junction photodiode is used since the standard CMOS process does not offer an intrinsic layer necessary for a p-i-n diode. The thin depletion region of the p-n junction diode results in only a fraction of the incident photons being captured in the depletion region, and it is here where there is a large electric field to assist the separation of the photo generated electron-hole pairs and their sweeping out of the depletion region. Photo generated minority carriers created outside the depletion region either recombine elsewhere and therefore do not contribute to the photocurrent or must diffuse to the depletion region to contribute to the photocurrent. This is a slow process and results in poor quantum efficiency (i.e., the number of electrons contributing to the photocurrent per incident photon) and, more importantly, a slow component of photocurrent which

compromises speed. That is, in response to an incident light impulse, the photocurrent exhibits a fast component that rises and decays rapidly and which is superimposed on a slow component that decays slowly and forms a "tail".

The use of transistors as detectors is unsatisfactory at high frequencies, predominantly because of such unwanted "tails" in detected pulses caused by the slow-moving diffusion of carriers generated in the base of the transistor.

Currently, there are two approaches to overcoming this problem:

First, fast photodiodes employing compound semiconductor technology are hybridised with silicon CMOS. This typically requires flip-chip solder bump technology. The disadvantage of this approach is that the parasitic capacitance of the large solder bumps compromises speed; the solder bonds and the different thermal expansion coefficients of the chips reduce reliability and yield and hence increase cost. Also, the area taken up by the bonding pads prevents the achievement of small photo detector array pitches (circa 10 um) which are thought to be required for high-density optoelectronic interconnects for integrated circuits applications.

Secondly, spatially modulated light detectors have been provided. The requirement is to remove the slow current component by detecting the difference current between interdigitated electrodes on monolithically integrated

(CMOS) photodiodes. The disadvantages are a reduced quantum efficiency due to the interception of the light by the metal electrodes on the photo detector surface; the large photo detector area required increased receiver complexity and bit rates limited to in the region of 300 Mbit/s.

The present invention seeks to provide for an optoelectronic detector, and related circuit arrangement, exhibiting an advantage over known such detectors and circuits and particularly which allows for a relatively high quantum efficiency and related speed of operation.

According to one aspect of the present invention, there is provided a *p-i-n* photodiode comprising a reversed bias base-collector junction of a silicon based integrated HBT device.

Speed and quantum efficiency of such a device represents an improvement over currently available devices.

A Si/Ge HBT BiCMOS offers a process compatible photodiode that can include an intrinsic region. The emitter of the HBT structure is in fact omitted. The base acts as the p-layer, the collector acts as the intrinsic layer, and the sub-collector acts as the n-layer. The whole of the intrinsic region can be depleted by a reverse bias that its less than the structure's breakdown voltage. The width of this depletion region is well matched to the absorption length of light in Si-Ge at IR wavelengths compatible with VCSEL sources (0.8-1.0 um). This can lead to a high quantum efficiency and little diffusion component to the photocurrent. Moreover, the reverse biased parasitic diode between the sub-collector layer and the substrate sweeps

away any carriers generated by photons captured in that region further reducing the potential for a diffusion component to the current.

One aspect of the present invention relies on the use of the reversed biased base-collector junction of an integrated SiGe HBT as the detector. The base collector and subcollector layers of the HBT in question form the p-i-n layers of the photodiode detector. Advantageously, the device can be formed as part of a current AMS 0.8μm SiGe HBT foundry process. Instructions are given to the foundry engineers not to grow the emitter layer of the device.

The basic photodiode structure has a response extending to circa 40 Gbit/s. Currently the speed limitations are caused by the receiver circuitry although improvements can be expected through better circuit design and the use of reduced feature size processes.

According to another aspect of the present invention there is provided a monolithic semiconductor structure comprising a *p-i-n* photo diode formed of a reversed bias base-collector junction of an integrated HBT device and a transimpedence amplifier arranged to be driven by an output from the HBT device, the transimpedence amplifier including a negative feedback buffer.

An advantageous aspect is that the circuits required can be very simple, take up little chip area and have low-power dissipation and so enable the formation of high density arrays.

As mentioned, the output current from the photodiode device can be used to drive the base of another HBT connected to form of a transimpedance amplifier.

It should be appreciated that SiGe can prove to be a better choice than Si for use as a p-i-n photo diode operating at 850 nm because its absorption at this wavelength is almost an order of magnitude greater.

As will therefore be appreciated in order to minimise the tail effect, it is important that most, if not all, of the carriers are generated within the junction's depletion region. Increasing the depletion region width in this way also improves performance by ensuring that the carriers drift at, or close to, saturation velocity.

The invention is described further hereinafter, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a schematic perspective view of a SiGe HBT photo diode device employed within an embodiment of the present invention;

Fig. 2 illustrates a SiGe HBT for use in the present invention;

Fig. 3 illustrates a bandgap diagram for a SiGe HBT structure as employed in accordance with an embodiment of the present invention;

Fig. 4 is a first example of an equivalent small signal

diagram for a photo receiver embodying the present invention;

Fig. 5 is a circuit diagram of a monolithic device according to an embodiment of the present invention and comprising a photo resistor and a transimpedence amplifier;

Fig. 6 is a trace illustrating the dynamic resistance of the load illustrated in the circuit arrangement of Fig. 5;

Fig. 7 is a trace of the dynamic resistance of the feedback device employed within the circuit arrangement of Fig. 5;

Fig. 8 is a trace illustrating the photo receivers dynamic load as plotted against frequency;

Fig. 9 is a trace illustrating the transimpedence game of certain arrangements such as that illustrated in Fig. 5;

Fig. 10 illustrates a trace of the peak output voltage plotted against frequency of the circuit arrangement of Fig. 5; and

Figs. 11 and 12 illustrate traces of the transients in relation of the output circuit arrangement of Fig. 5 at point 5GHz and 1GHz respectively;

Fig. 13 is a circuit arrangement of a monolithic device including a photo receiver and transimpedence amplifier according to an alternative embodiment of the present invention;

Fig. 14 is a similar circuit diagram according to a yet further embodiment of the present invention;

Fig. 15 illustrates the transient response arising in relation to the circuit of Fig. 14;

Fig. 16 is a trace representing the AC analysis arising in relation to the circuit of Fig. 14;

Fig. 17 is a second example of an equivalent small signal diagram for a photo receiver embodying the present invention; and

Fig. 18 represents the bandwidth of a detector employing the photodetector of Fig. 17.

In accordance with a particularly advantageous aspect, the invention seeks to provide for a photo receiver design employing a small surface area, low power consumption, low heat dissipation and should be suitable for mass production and for operation at >1 GBps.

Turning first to Fig. 1, there is illustrated a schematic perspective view of a SiGe HBT photodiode which can be employed in accordance with the present invention. As noted, no emitter region need to be provided for the device and such emitter region is commonly omitted at the time of device formation. In Fig. 2 there is illustrated the general structure of a SiGe HBT for use in an embodiment of the present invention.

Fig. 3 illustrates a band gap diagram for the emitter, base and collector of the SiGe device and which, as is illustrated, includes a Ge doped region that extends only a relatively short distance into the collector region. While the advantages of the present invention can be achieved by means of such a silicon absorption layer device, particularly if wavelengths in the order of 650nm are considered and as is described in further detail later, it should be appreciated that an increased concentration of Ge in the collector region can lead to use at a wavelengths in the order of 850nm.

For ease of understanding of the calculations that follow, and that relate to a SiGe absorption layer for use with wavelengths in the order of 850nm, Fig. 4 illustrates an equivalent small signal model 10 disposed between a cathode connection 12 and anode connection 14 and which comprises parallel connected elements current source Iph 16, capacitors C_j 18, an ideal-value diode 20 and resistor Rsh 22. These parallel connected elements being connected in the series with a resistor Rs24.

In a preferred embodiment, the diode's dimensions have been calculated to accept a typical IR LASER beam (Beam Area = $10\mu m^2$, $P\lambda$=1.25mW). The depletion region width required in order to minimise the "tail" effect can be calculated as follows,

$$W \geq \frac{1}{\alpha_{(850nm)}}$$

SiGe has higher absorption at 850nm than Si, Table 1.

SiGe has higher absorption at 850 nm than Si, Table 1.

$\alpha(850\ nm)_{Si} = 1x10^5$	$\alpha(850\ nm)_{SiGe} = 8x10^5$

Table 1. Absorption of Si and SiGe at λ=850nm.

This property helps reduce the necessary depletion region width needed,

$$W = \frac{1}{8\times10^5} = 1.25\mu m.$$

The minimum electric field required to achieve saturation velocity in SiGe is $1x10^7$ V/m. At 1.25 μm, the total reverse bias voltage (including the built-in potential of 0.97V) required is given by,

$$V_R = 1x10^7 \times 1.25x10^{-6} = 12.5V$$

Therefor, the reverse bias voltage required ≥ 11.5V and is limited by the junction's breakdown voltage (14V).

Using Poisson's equation, for a given total reverse bias voltage of 12.5 V, the depletion width can be calculated as follows,

$$x_d = \sqrt{\frac{2\varepsilon_o\varepsilon_r(V_R + V_{bi})}{qN_D}} \qquad x_d = \sqrt{\frac{2\times8.85\times10^{-12}\times12.1\times12.5}{1.6\times10^{-19}\times1\times10^{22}}} = 1.29\mu m$$

This biasing arrangement results in a depletion thickness almost equal to the collector depth. this greatly minimizes the unwanted 'tails' in the output pulses.

The carrier transit time in the depletion region is given by,

$$\tau_t = \frac{x_d}{2v_{Sat}} = \frac{1.29\times10^{-6}}{2\times1\times10^{7}} = 6.45\times10^{-15}s$$

The junction capacitance and series resistance are determined as follows,

$$C_j = \frac{\varepsilon_o\varepsilon_r A}{x_d} = \frac{8.85\times10^{-12}\times12.1\times1\times10^{-11}}{1.29\times10^{-6}} = 0.83\times10^{-15}F$$

$$R_S = \rho\frac{l}{A} = 6.25\times10^{-6}\times\frac{1.6\times10^{-6}}{1\times10^{-11}} = 1\Omega$$

Given the large depletion width, a quantum efficiency of 90% can be expected (assuming appropriate anti-reflection coatings) and the diode's responsivity obtained,

$$R = \frac{\eta q}{h\nu} = \frac{0.9\times1.6\times10^{-19}}{2.34\times10^{-19}} = 0.62A/W$$

In this application, the light source is provided by a VCSEL diode with an output power of 1.25 mW, positioned close to the detector (no power loss from transmitter to receiver is assumed).

Thus, the photo-generated current for an incident power of 1.25 mW is as shown,

$$I_{Ph} = R\times P_\lambda = 0.62\times1.25\times10^{-3} = 775\times10^{-6}A$$

Parameter	Value
N_D	$1x10^{22}$ m^{-3}
N_A	$1x10^{24}$ m^{-3}
V_{Break}	14 V
V_R	12.5 V
V_{bi}	0.97 V
x_n	1.29 µm
x_p	0.1 µm
x_{tp}	1.6 µm
Surface Area	5 x 2 μm^2
v_{Sat}	$1x10^{7}$ ms^{-1}
P_λ	1.25 mW

Detector Junction Parameters

Current from the reversed biased junction detector feeds a transimpedance amplifier formed by a HBT common-emitter amplifier and a MOSFET negative feed back buffer as illustrated in Fig. 5.

Fig. 5 illustrates a small signal equivalent circuit 10 such as that illustrated with reference to Fig. 4, and, as mentioned above, the current produced is arranged to feed the transimpedence amplifier formed by the HBT common emitter amplifier Q1 which is itself connected to a MOSFET load M1, and which arrangement also includes a MOSFET negative feedback buffer M2.

$$I_B = 28.35\ \mu A,\ I_C = 210.8\ \mu A,\ V_{CQ} = 3.278V$$

The circuit's total power consumption $\cong 210.8\ \mu A \times 5V \cong 1\ mW$

The emitter's series emitter is approximated by,

$$r_e = \frac{0.027}{211 \times 10^{-6}} = 128\Omega$$

The DC current gain is obtained from,

$$\beta = \frac{I_C}{I_B} = \frac{210.8 \times 10^{-6}}{28.35 \times 10^{-6}} = 7.44x$$

The dynamic resistances of both the MOSFET load and feedback device can be obtained by simulation as shown in Figs. 6 and 7. With reference to Fig. 5, Fig. 6, shows the dynamic load resistance of device M_1 and Fig. 7 the dynamic load

resistance of device M_2.

Fig. 7 illustrates a trace of the dynamic feedback resistance of device M_2 of Fig. 5.

The amplifier's voltage gain is given by.

$$A_v = \frac{R_{Load}}{r_e} = \frac{4000}{128} = 31.3x$$

The diode's load resistance can also be obtained by simulation as shown in Fig. 7 and calculated as below,

$$R_L = \frac{R_F}{1 + A_v} = \frac{13000}{1 + 31} \approx 400\Omega$$

The diode's dynamic load Vs Frequency is illustrated in Fig. 8.

The detector junction's bandwidth is dependent upon its junction capacitance and the load resistance used to convert the detected current into voltage.

$$BW = \frac{1}{2\pi R_L C_J} = \frac{1}{2 \times 3.142 \times 450 \times 0.83 \times 10^{-15}} = 426 \times 10^{9}\ Hz$$

The HBT's model parameters are given in the table below.

Paramater	Value
Emitter Length	2 μm
Emitter Width	0.8 μm
RB	350 Ω
RE	40 Ω
RC	100 Ω
CJC	7.5 fF
CJE	3.3 fF
VAF	100 V
VJE	0.91 V
VJC	0.67 V
BR	5
BF	8
IKF	2 mA
TF	4.3 pS
EG	0.97 eV

Table 3, AMS HBT NPN111 Model Parameters.

The AMS foundry's own BSIMv3 MOSFET models are used, dimension and resistance values are given in the table below.

Parameter	MOSFET 1 Values	MOSFET 2 Values
Emitter Length	1μm	1μm
Emitter Width	6μm	1μm
Equivalent DC Resistance	8170 Ω	150 KΩ
Equivalent Dynamic Resistance	4 KΩ	13 KΩ

AMS NMOS Dimensions.

The circuit was simulated using MiCROSIM's PSPICE A/D package's transient analysis. A pulse generator was used to simulate the input photocurrent.

The simulated peak output for a given peak input current of 775μA, over the entire frequency of operation, was obtained and graphs of transimpedance gain Vs Frequency and peak output voltage Vs frequency were plotted as illustrated in

Figs. 9 and 10 respectively.

The measured bandwidth is much less than that calculated for the photoddector.

The overall bandwidth is reduced by parasitic capacitances in the M_1 load, M_2 feedback resistance and the HBT.

Although intended for operation to 2 Gbps, the amplifier's capability to switch a light CMOS load to above a + 1.5V logic threshold at greater than 2 Gbps is shown in Fig. 11 and with the transient analysis of the output at 0.5 GHz and at 1 GHz being shown in Figs. 11 and 12.

Should greater sensitivity be required, one or more CMOS buffer amplifier stages (M3x and M4x), of preset gain, can be added to the design as shown in Fig. 13.

In Fig. 13, there is again illustrated an equivalent small signal model 11 for the photo receiver device again driving a transimpedence amplifier Q2 connected to a negative feedback MOSFET buffer M2 and a MOSFET load M1 but, as mentioned, an additional two CMOS buffer amplifier stages M3A/B and M4A/B also being provided.

Fig. 14 illustrates a further variant of the photo receiver circuit which advantageously employs inverter elements M1 and M2 which serve to reduce the charge/discharge time as seen by the photodiode.

Figs. 15 and 16 illustrate the transient response, and AC

analysis respectively of the alternate circuit arrangement of Fig. 14.

It is also viable to operate the detector at 650nm and with the absorption layer comprising Si since the absorption of Si at 650nm is almost a factor of ten greater than that at 850nm, and this therefore improves the photodiode's responsivity. Although not presently available, red VCSEL sources for 650-70nm and are likely to represent appropriate sources.

Thus, although the foundry process employed at manufacture could be varied so as to increase the Ge concentration in the collector region by adding a custom diffusion step to the standard process, and so as to greatly improve the detector's absorption for operation between 650 and 850nm as discussed previously, operation at wavelengths in the order of 650nm is also available as explained in the analysis below.

Some of the formulae used for the calculation of parameters in the simulation have been taken from a PSPICE model in order to ensure the smallest margins of error. The results of this analysis are as follows and arise from the same calculations and simulations noted above for operation with 850nm source.

At an input power of 1mW, the following results arise.

	Area = 22·μμ m	η = 0.6	IS = 0.027·10^-16
CJO := 1.071 fF	Cj = 1.859·fF	Responsivity = 0.314 A/W	
	Rs = 2.4·10^3	IΦ = 313.911·μA	
	VR = 14	Xd = 1.362·μm	
	τt = 6.808·pS	BW = 85.601·GHz (for 1 KOhm resistive load)	

However, since it is unlikely that a loss-less link will be implemented, it is necessary to include a minimum-6dBm (75%) power loss at the receiver for the following point-to-point link simulations. The re-calculated values for the new input power of 0.25mW are listed below.

	Area = 22·μμ m	η = 0.6	IS = 0.027·10^-16
CJO := 1.071 fF	Cj = 1.859·fF	Responsivity = 0.314 A/W	
	Rs = 2.4·10^3	IΦ = 78.478·μA	
	VR = 14	Xd = 1.362·μm	
	τt = 6.808·pS	BW = 85.601·GHz (for 1 KOhm resistive load)	

Using model parameters from the foundry process PSPICE model files, it is possible to produce a new PSPICE photodiode model 110 for use in PSPICE simulations and this is illustrated in Fig. 17. The arrangement of the elements of the model is generally similar to that in Fig. 4 but here: resistor 124 has a value of 0.0024 Ohms; resistor 122 has a value in excess of 100 MOhms; diode 120 remains ideal; capacitor 118 has a value of 1.071 f and the current source 116 produces a current in the region of 70μA.

Using this model, PSPICE simulation can be used to verify the detector's bandwidth (~80GHz or 160 GBps) obtained by analysis and a trace of which is illustrated in Fig. 18.

As noted, the resultant photo-detected current is 78μA and this value can be readily used to drive a low input impedance/high gain monolithic transimpedance amplifier, fabricated using MOSFET's and HBT's from the same BiCMOS process.

Thus, as will be appreciated, while SiGe's higher absorption coefficient at IR frequencies enables the SiGe diode to outperform a similarly sized biased Si device, Si nevertheless offers a viable option for wavelengths in the order of 650nm. At wavelengths in the order of 850nm, without the reduction in the necessary depletion width attributable to SiGe's absorption of IR, the bias voltage required to enable the device to operate correctly would have been larger than the device's reverse breakdown voltage in this case (e.g. a Si device in this process would not work). Even if Si devices are fabricated, in other processes, that can take the extra bias required to achieve a similar level of performance, the replacement of any given Si diode with a similar SiGe device (for a set bias) will always be an improvement.

Advantageously the overall cost of fabricating SiGe devices is far less than that of GaAs devices as it approximates to the cost of Si fabrication.

At the wavelengths mentioned, the direct integration of this

photo detector diode in any design will inevitable result in a reduction complexity cost and of the required wafer space when compared with designs implemented using a flip-chip bonded (group III-V material) diode and an increase in bandwidth when compared with designs based on Si diodes/phototransistors.

CLAIMS

1. A photo receiver comprising a *p-i-n* photodiode formed of a reversed biased base-collector junction of a silicon based integrated HBT device

2. A photo receiver as claimed in Claim 1, wherein the collector of the photodiode is in at least part silicon collector.

3. A photo receiver as claimed in Claim 2, wherein the collector comprises a substantially silicon collector.

4. A photo receiver as claimed in any one of Claims 1-3, and comprising a SiGe *p-i-n* device.

5. A photo receiver as claimed in Claim 4, wherein the Ge extends at least partially into the collector.

6. A photo receiver as defined in any one of Claims 1-5, wherein the photodiode is derived from an HBT structure formed without an emitter.

7. A photo receiver as claimed in any one of Claims 1-6 and arranged with an output connected to drive a transimpedence amplifier.

8. A photo receiver as claimed in Claim 7, wherein the transimpedence amplifier comprises a HBT-compatible device.

9. A photo receiver as claimed in Claim 7 or 8, wherein the transimpedence amplifier comprises a HBT common-emitter amplifier and further includes a negative feedback buffer.

10. A photo receiver as claimed in Claim 9, wherein the negative feedback buffer comprises a MOSFET negative feedback buffer.

11. A photo receiver as claimed in any of Claims 7-10, and including at least one CMOS buffer amplifier stage.

12. A photo receiver as claimed in any one of Claims 7-11, and formed as a monolithic structure.

13. A monolithic semiconductor structure comprising a *p-i-n* photodiode formed of a reversed bias base-collector junction of an integrated HBT device and a transimpedence amplifier arranged to be driven by an output from the HBT device, the transimpedence amplifier including a negative feedback buffer.

14. A monolithic structure as claimed in Claim 13, provided with a load device.

15. A monolithic structure as claimed in Claim 13 or 14 and including a buffer amplifier.

16. A photo receiver substantially as hereinbefore described with reference to, nd as illustrated in, any one or more of the accompanying drawings.

17. A monolithic semiconductor structure comprising a *p-i-n* photodiode and a transimpedence amplifier and substantially as hereinbefore described with reference to, and as illustrated in, any one or more of the accompanying drawings.

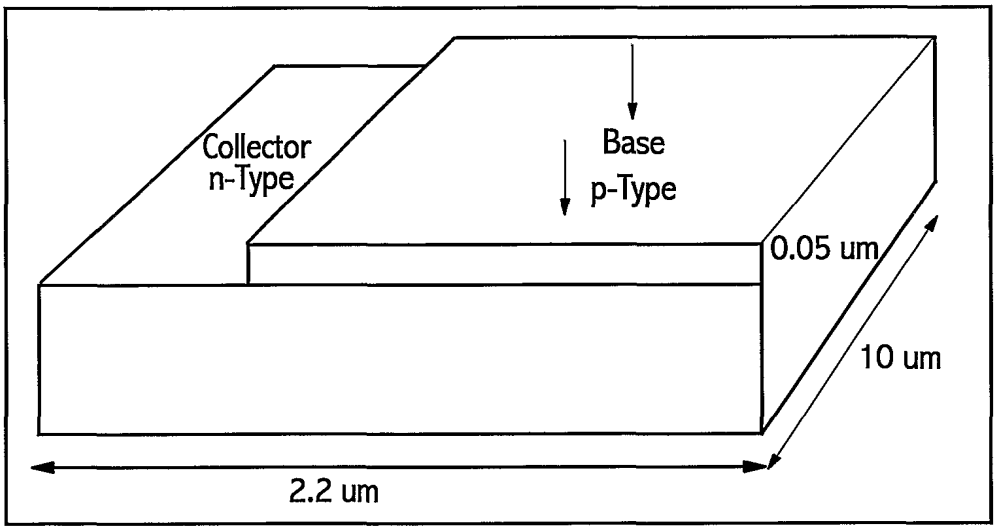
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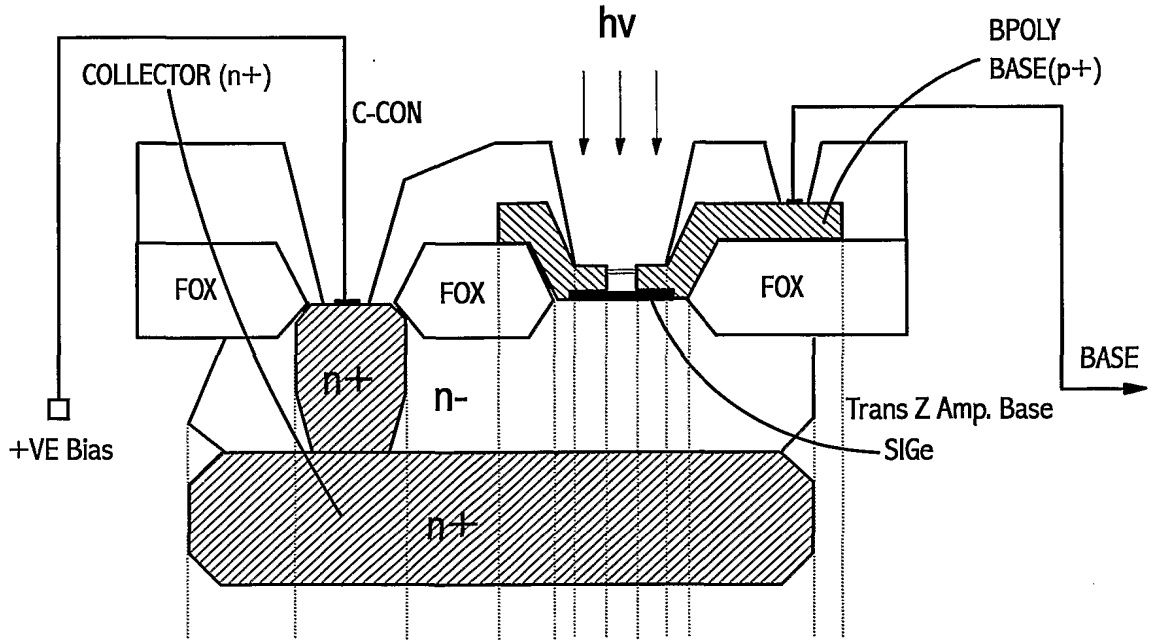
FIG.1.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SIGe
+VE Bias
n+

FIG.2.

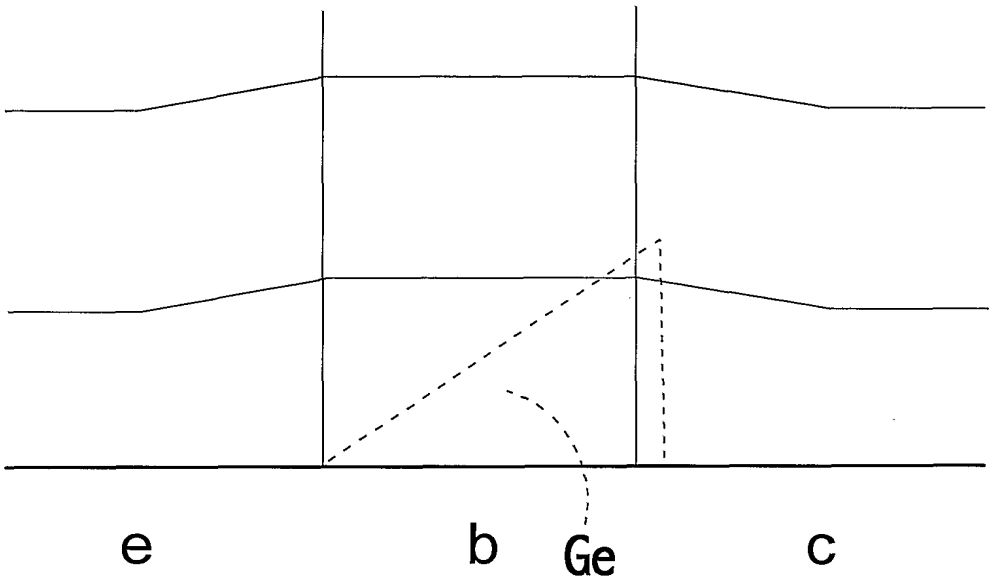

FIG.3.

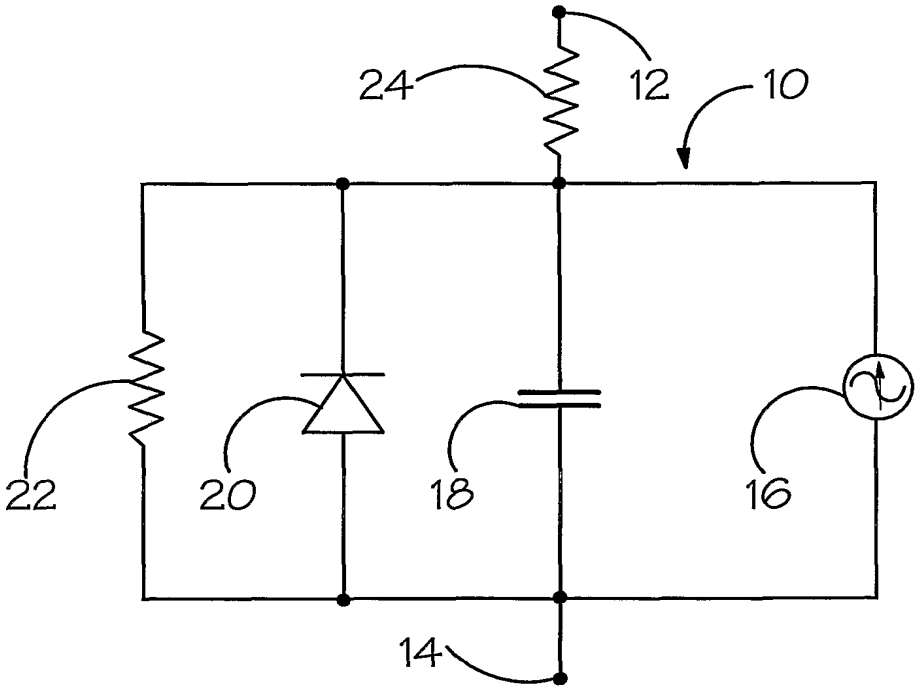

FIG.4.

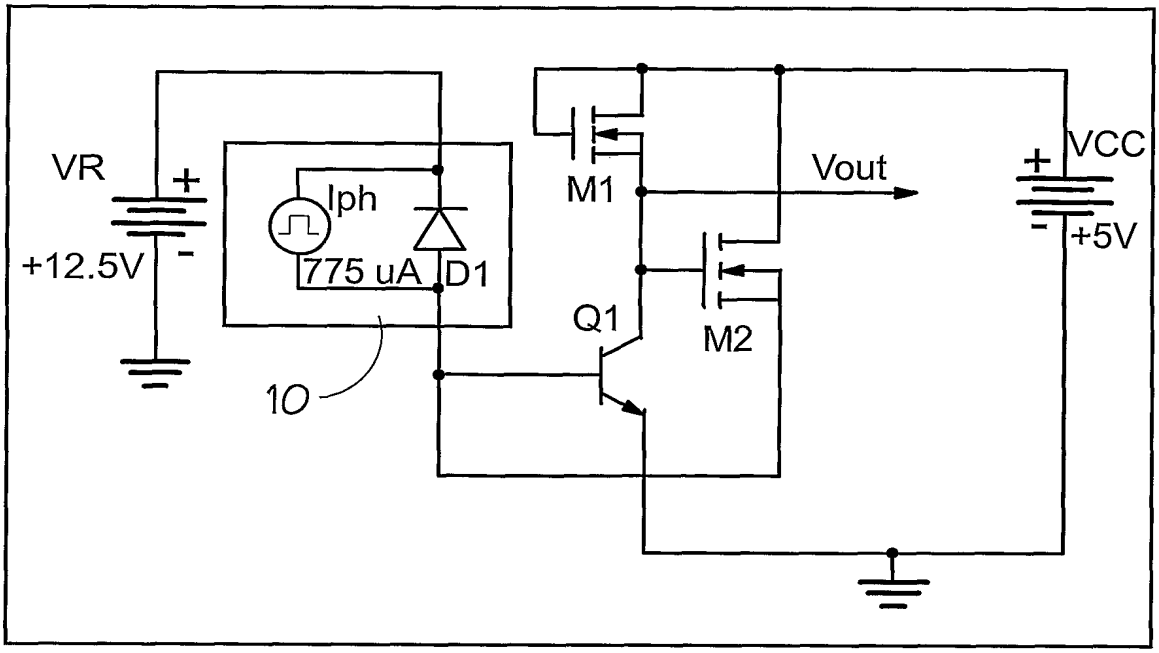
VR
+12.5V
Iph
775 uA
D1
10
M1
Q1
M2
Vout
VCC
+5V

FIG.5.

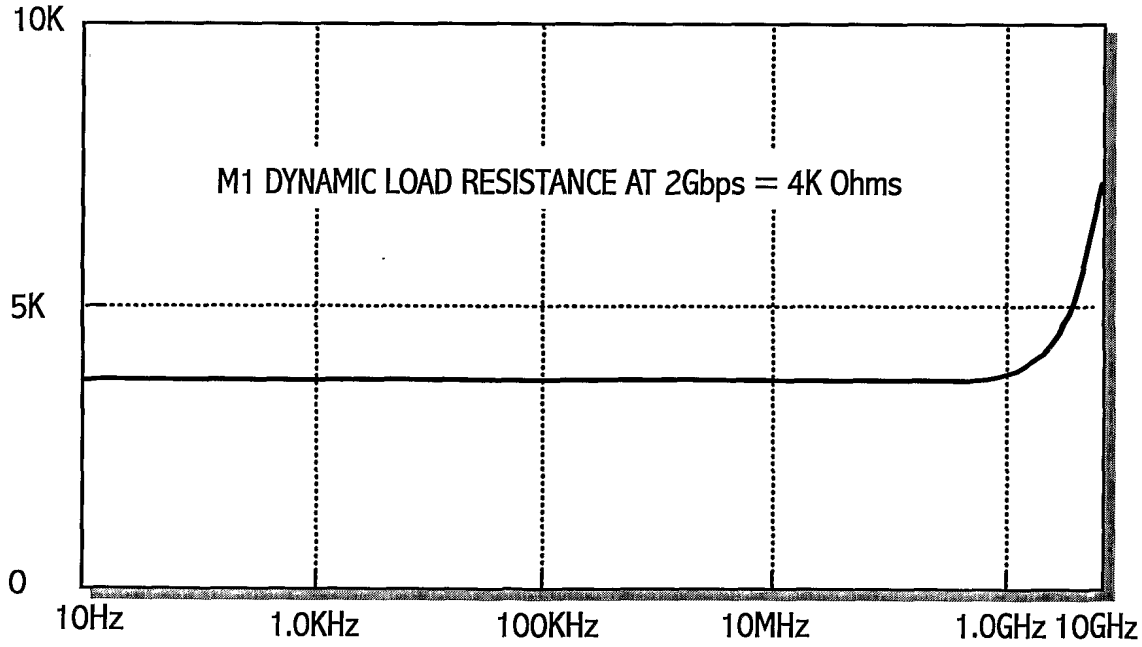
10K
5K
0
M1 DYNAMIC LOAD RESISTANCE AT 2Gbps = 4K Ohms
10Hz
1.0KHz
100KHz
10MHz
1.0GHz 10GHz

FIG.6.

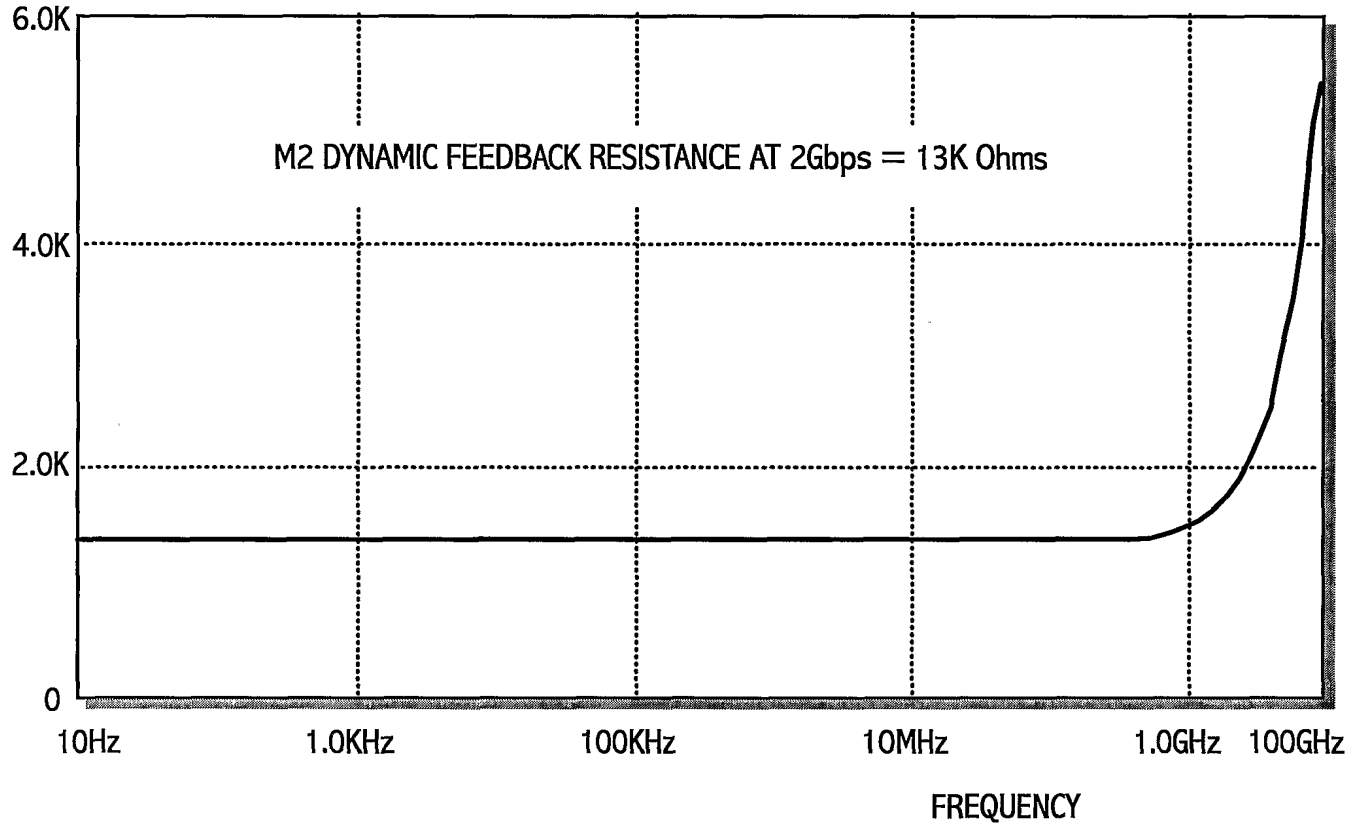
6.0K
4.0K
2.0K
0
M2 DYNAMIC FEEDBACK RESISTANCE AT 2Gbps = 13K Ohms
10Hz
1.0KHz
100KHz
10MHz
1.0GHz
100GHz
FREQUENCY

FIG.7.

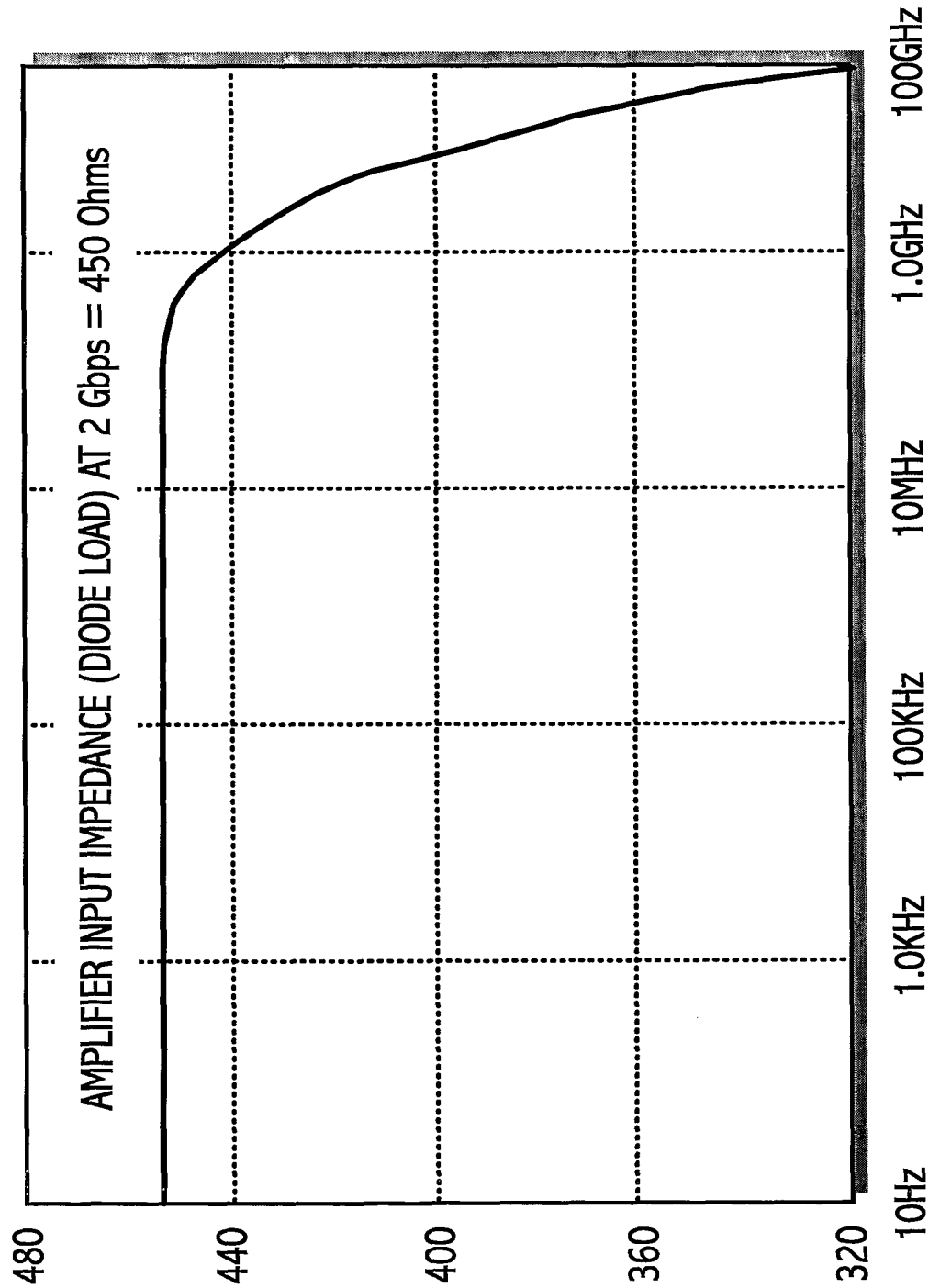
AMPLIFIER INPUT IMPEDANCE (DIODE LOAD) AT 2 Gbps = 450 Ohms
480
440
400
360
320
10Hz
1.0KHz
100KHz
10MHz
1.0GHz
100GHz
FREQUENCY
a v(Q1:b) / (I(D1) + I(IPh))

FIG.8.

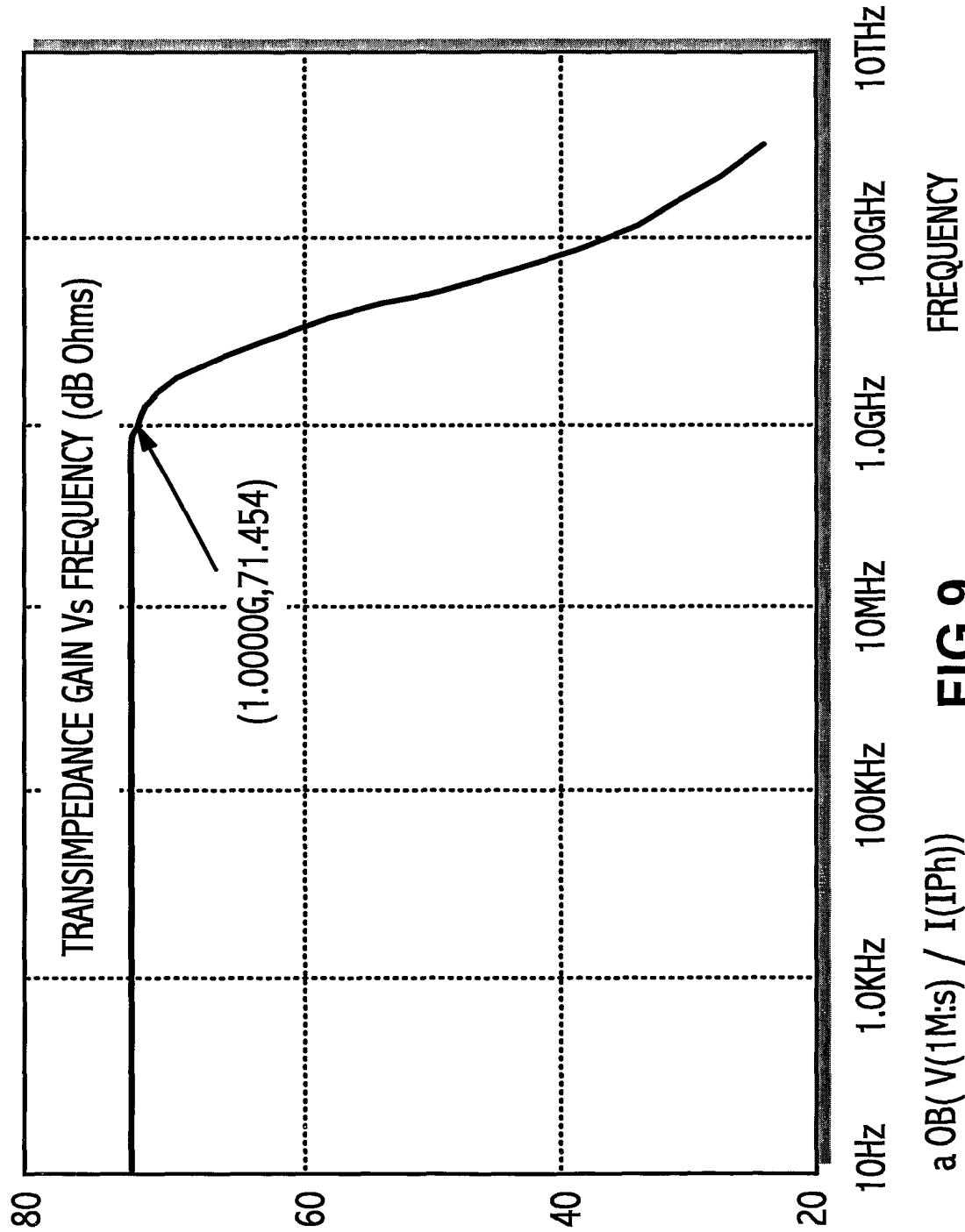
TRANSIMPEDANCE GAIN Vs FREQUENCY (dB Ohms)
(1.0000G,71.454)
80
60
40
20
10Hz
1.0KHz
100KHz
10MHz
1.0GHz
100GHz
10THz
FREQUENCY
a OB(V(1M:s) / I(IPh))

FIG.9.

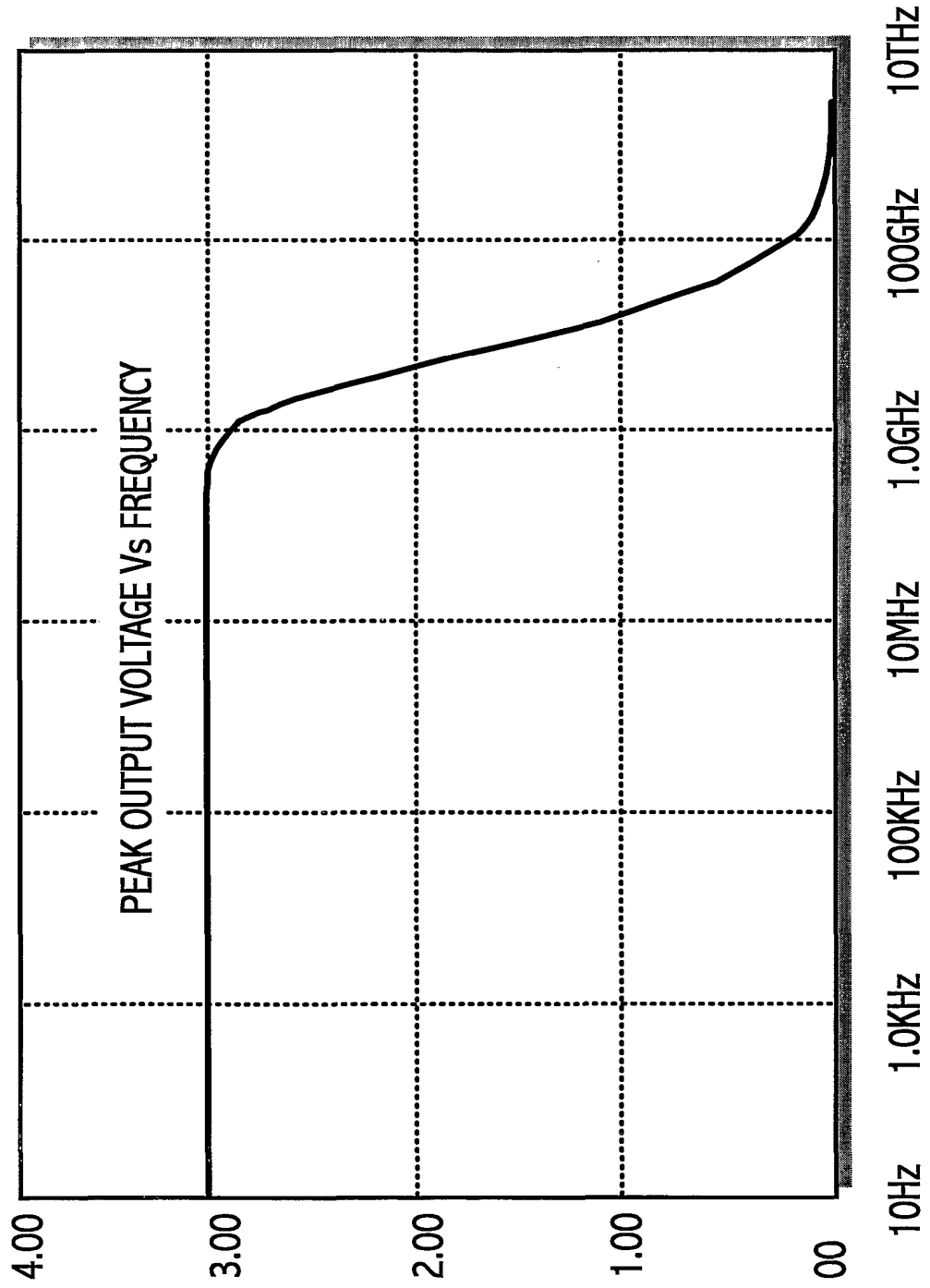
PEAK OUTPUT VOLTAGE Vs FREQUENCY
4.00
3.00
2.00
1.00
00
10Hz
1.0KHz
100KHz
10MHz
1.0GHz
100GHz
10THz
FREQUENCY
a v(Q1:c)

FIG.10.

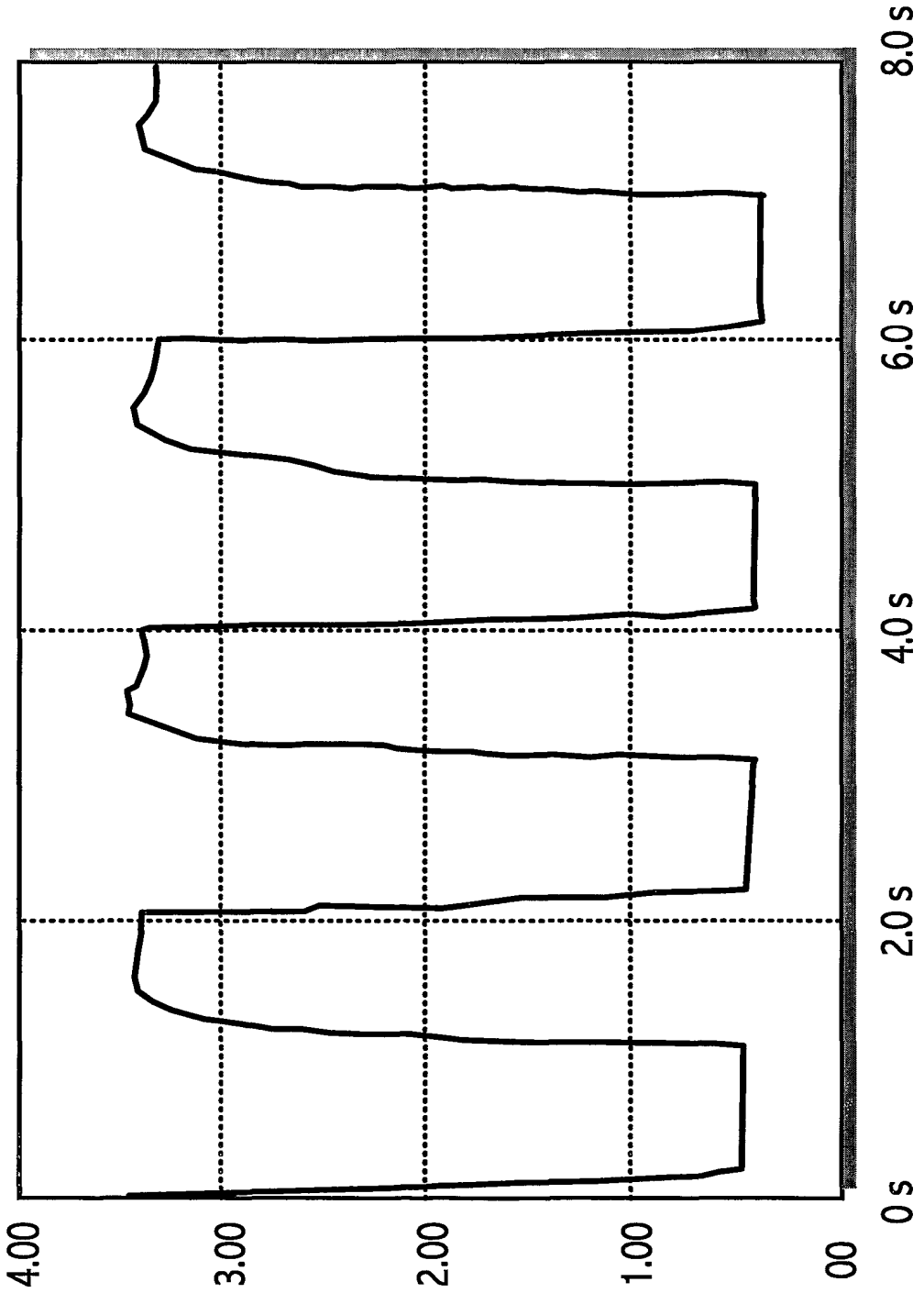

FIG.11.

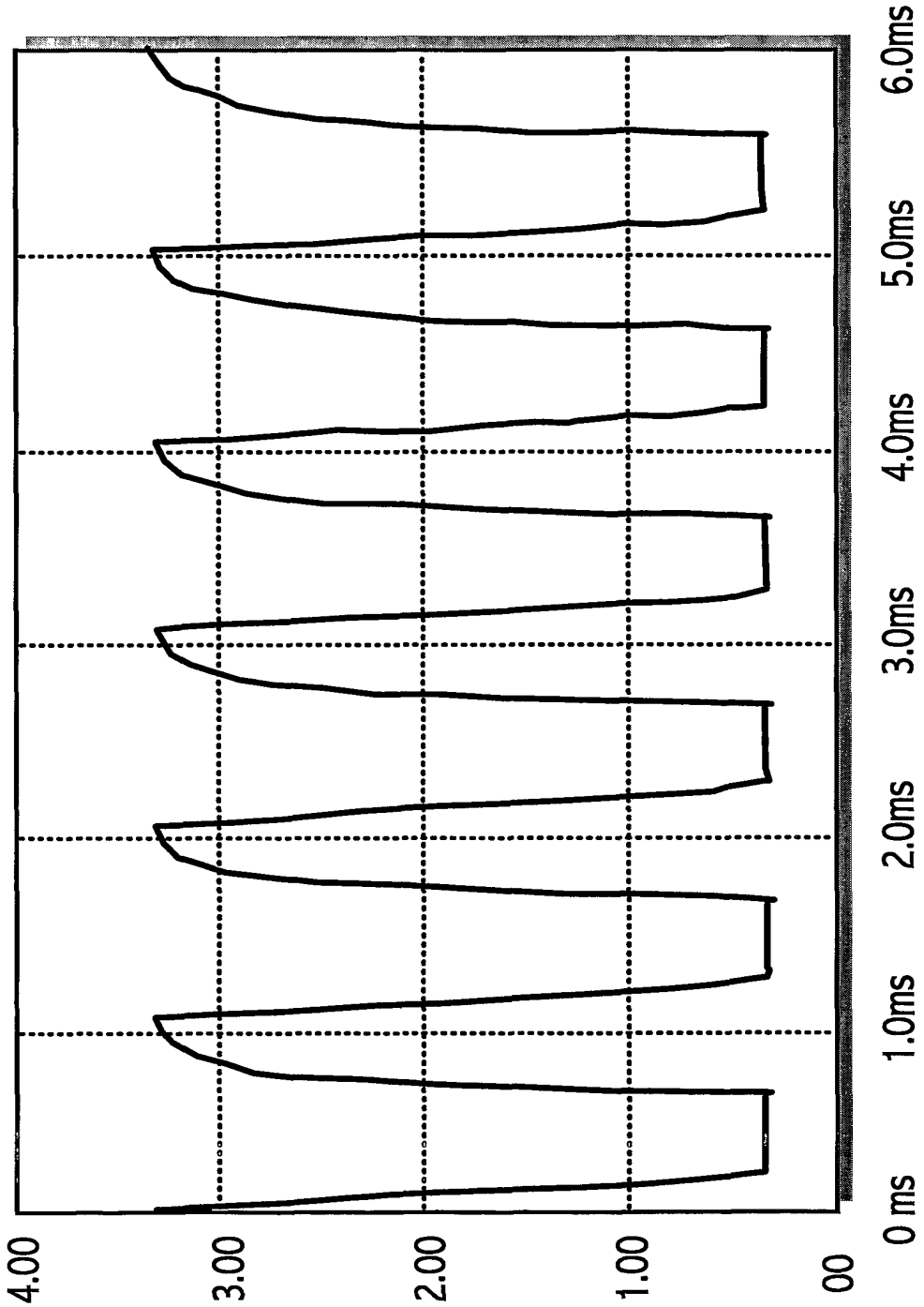
4.00
3.00
2.00
1.00
00
0 ms
1.0ms
2.0ms
3.0ms
4.0ms
5.0ms
6.0ms
TIME
a V(Q1:c)

FIG.12.

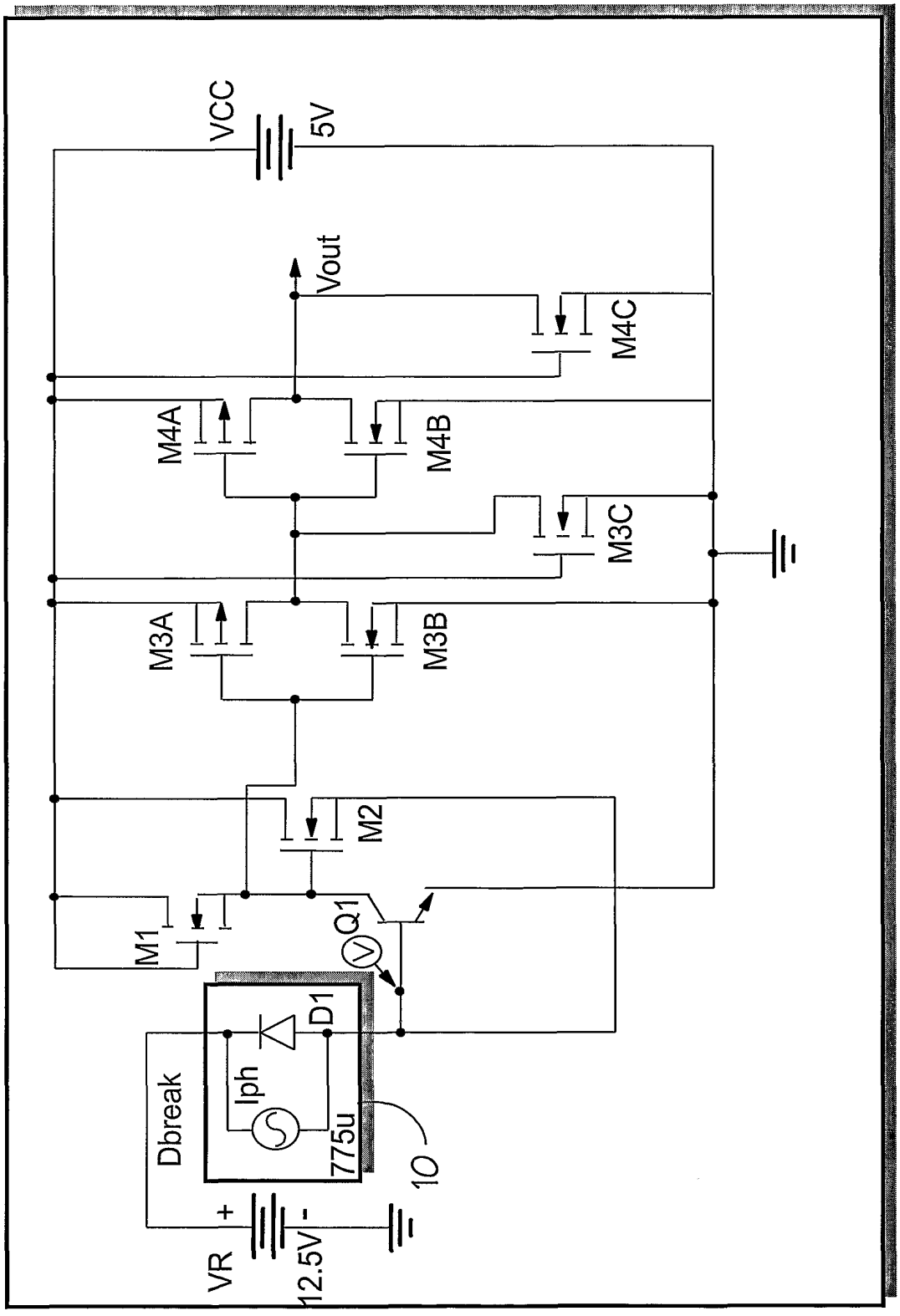
VCC
5V
Vout
M4C
M4A
M4B
M3C
M3A
M3B
M2
M1
Q1
D1
Iph
Dbreak
775u
10
VR
12.5V
+
-

FIG.13.

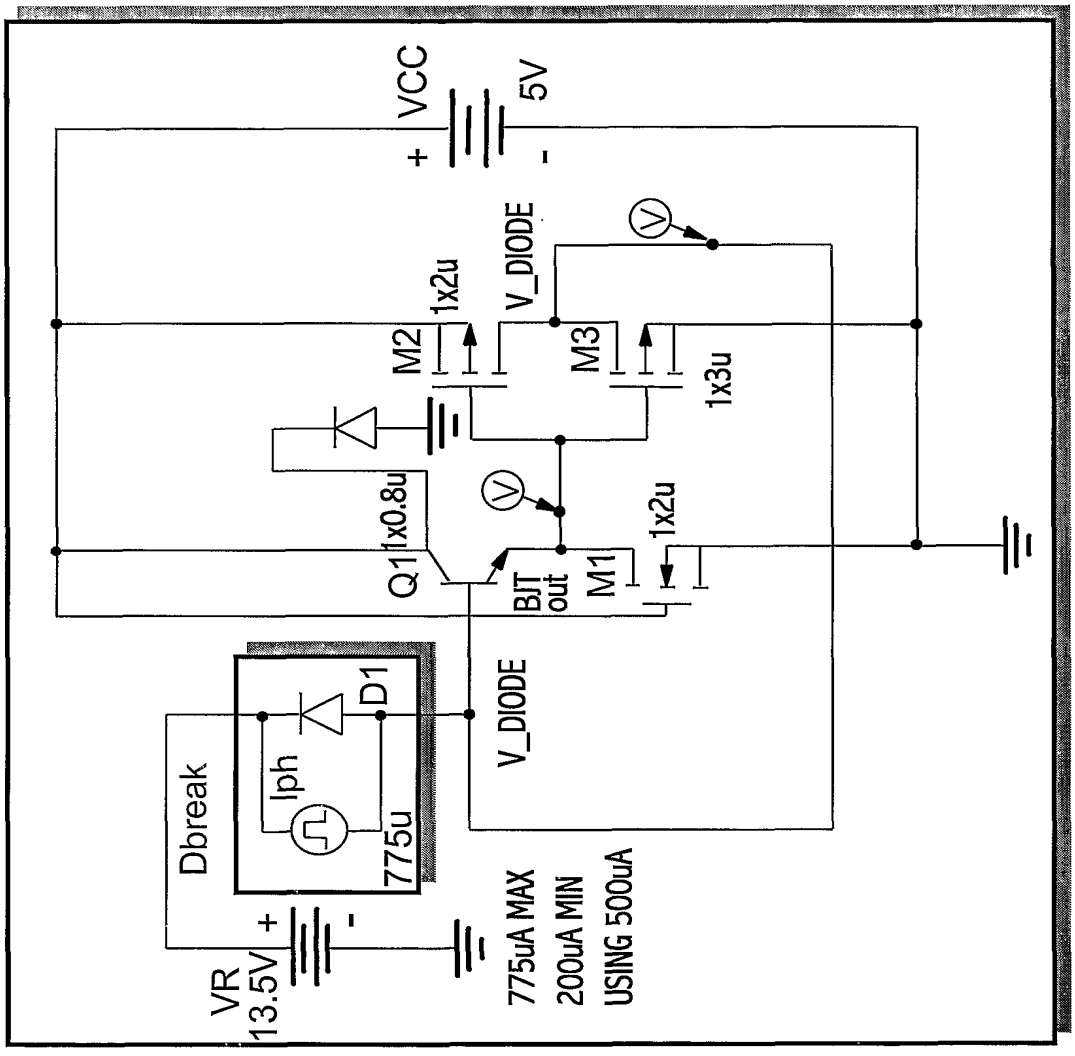
VCC
5V
V_DIODE
M2
1x2u
M3
1x3u
1x0.8u
Q1
BJT out
M1
1x2u
D1
Dbreak
Iph
775u
V_DIODE
VR
13.5V
775uA MAX
200uA MIN
USING 500uA

FIG.14.

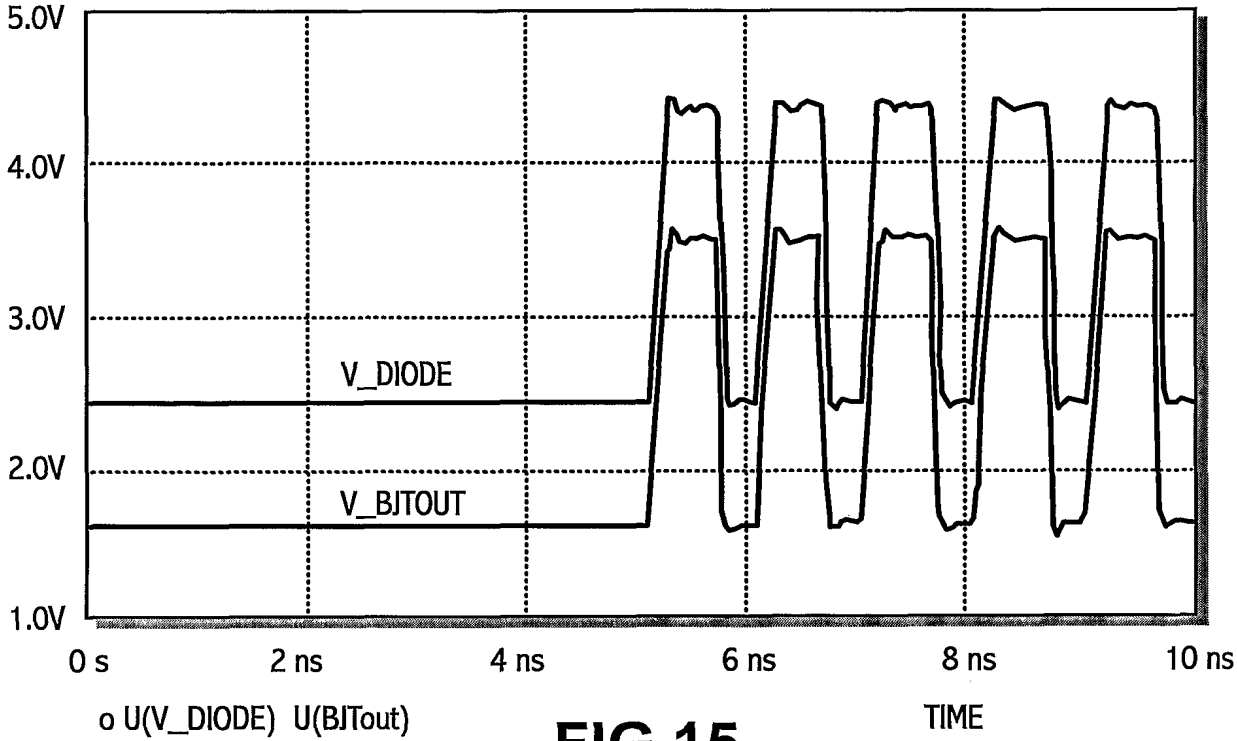
5.0V
4.0V
3.0V
2.0V
1.0V
V_DIODE
V_BJTOUT
0 s
2 ns
4 ns
6 ns
8 ns
10 ns
o U(V_DIODE) U(BJTout)
TIME

FIG.15.

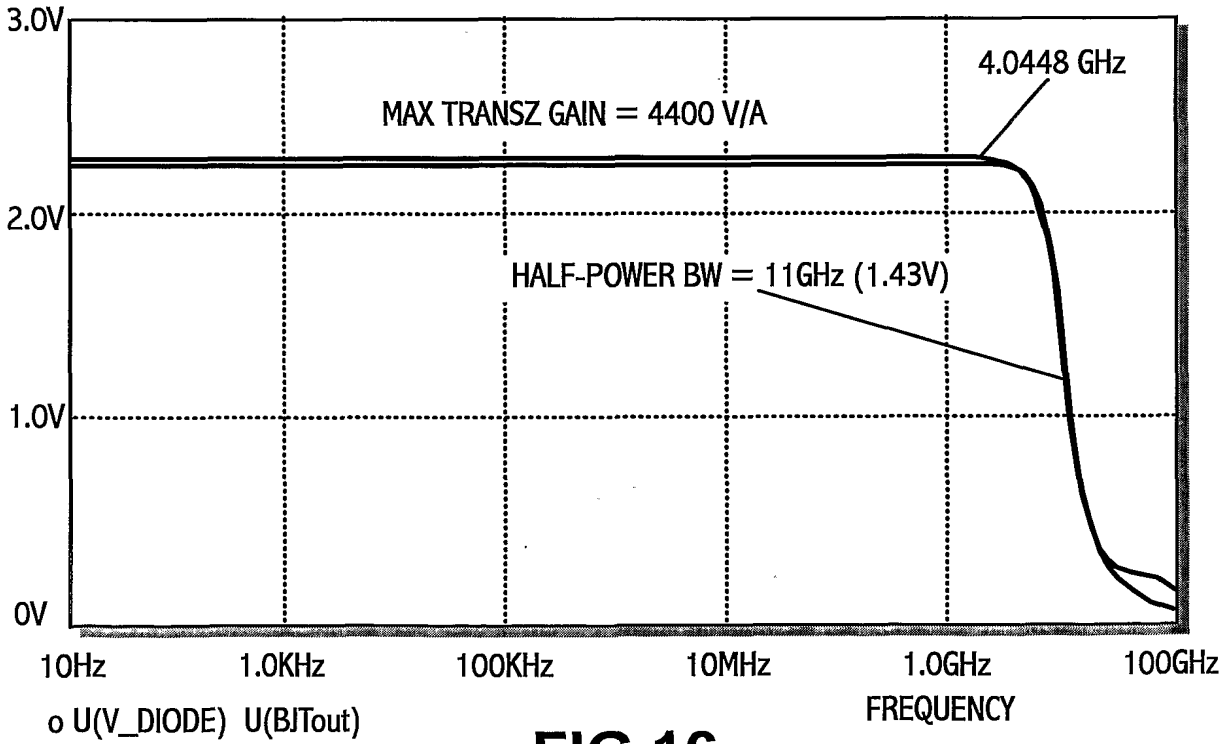
3.0V
2.0V
1.0V
0V
4.0448 GHz
MAX TRANSZ GAIN = 4400 V/A
HALF-POWER BW = 11GHz (1.43V)
10Hz
1.0KHz
100KHz
10MHz
1.0GHz
100GHz
o U(V_DIODE) U(BJTout)
FREQUENCY

FIG.16.

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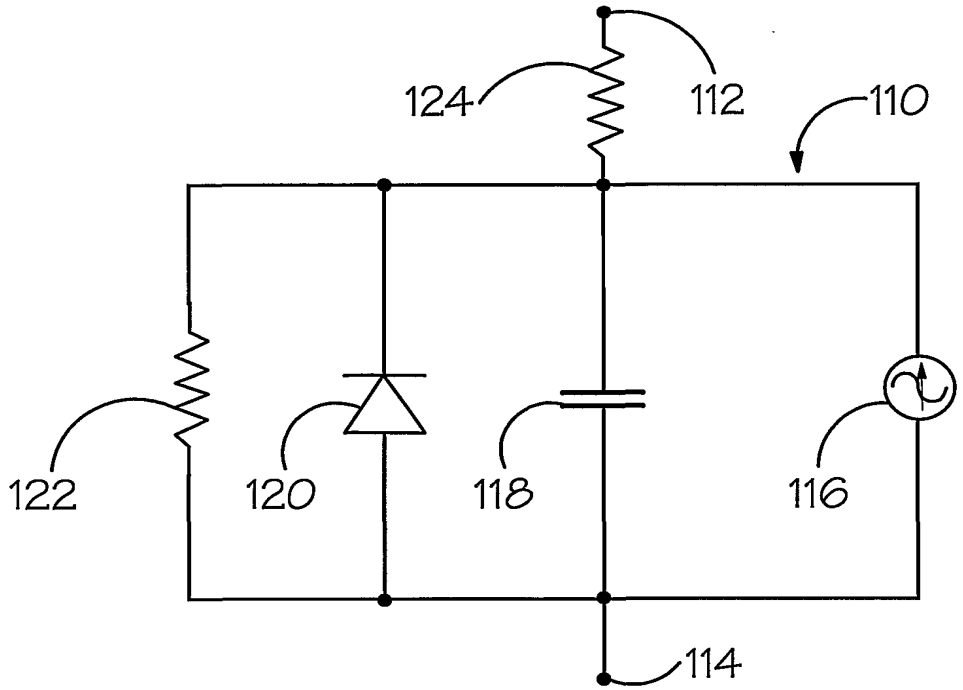

FIG.17.

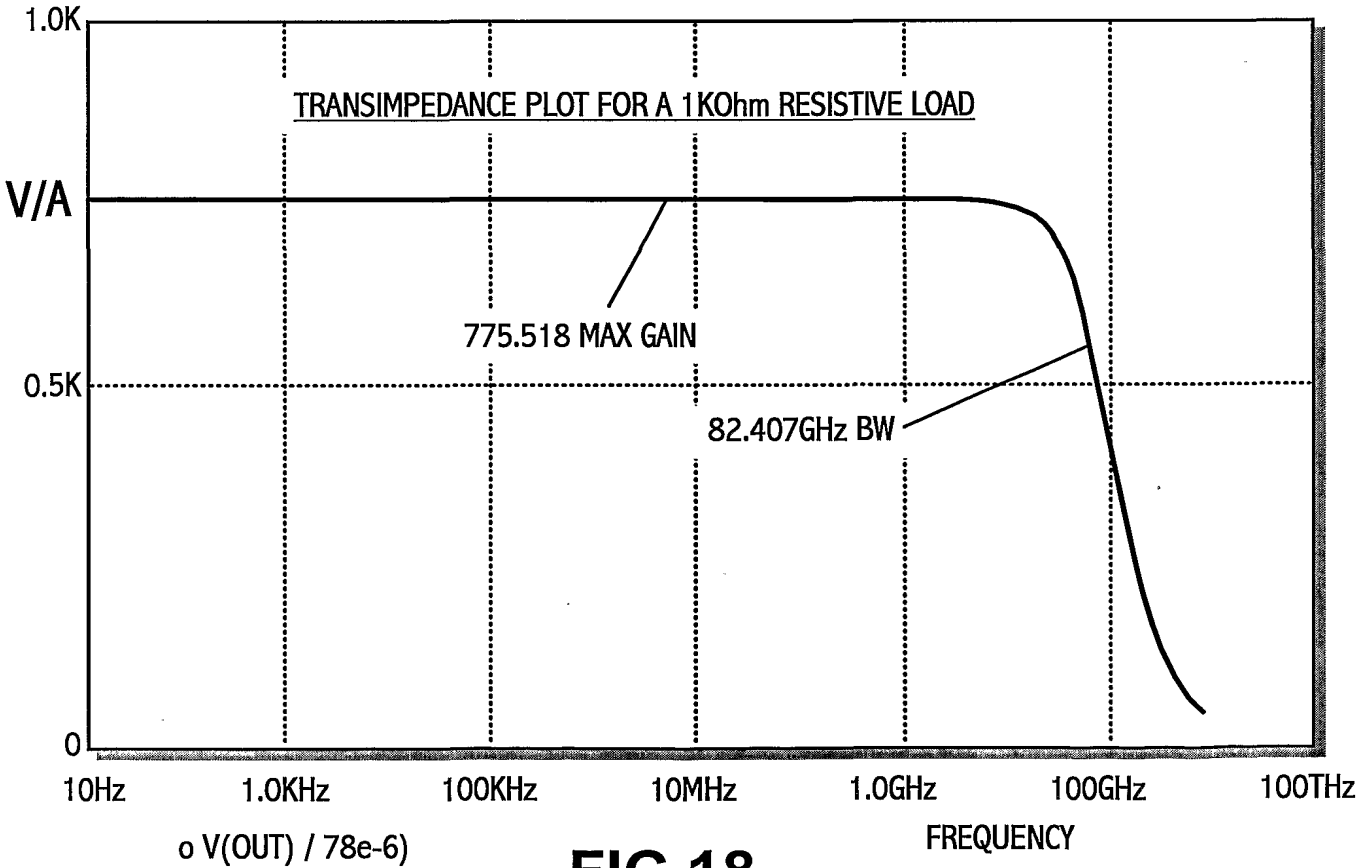

FIG.18.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 01/05527

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L31/105 H01L27/144

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	RIEH J-S ET AL: "Monolithically integrated SiGe/Si PIN-HBT front-end transimpedance photoreceivers" HIGH SPEED SEMICONDUCTOR DEVICES AND CIRCUITS, 1997. PROCEEDIINGS., 1997 IEEE/CORNELL CONFERENCE ON ADVANCED CONCEPTS IN ITHACA, NY, USA 4-6 AUG. 1997, NEW YORK, NY, USA,IEEE, US, 4 August 1997 (1997-08-04), pages 322-331, XP010264384 ISBN: 0-7803-3970-3 the whole document --- -/--	1-17

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 May 2002	13/05/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Werner, A

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 01/05527

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	MASUDA T ET AL: "40 Gb/s analog IC chipset for optical receiver using SiGe HBTs" SOLID-STATE CIRCUITS CONFERENCE, 1998. DIGEST OF TECHNICAL PAPERS. 1998 IEEE INTERNATIONAL SAN FRANCISCO, CA, USA 5-7 FEB. 1998, NEW YORK, NY, USA,IEEE, US, 5 February 1998 (1998-02-05), pages 314-315,454, XP010278667 ISBN: 0-7803-4344-1 the whole document	1
A	YAMAMOTO M ET AL: "SI-OEIC WITH A BUILT-IN PIN-PHOTODIODE" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE INC. NEW YORK, US, vol. 42, no. 1, 1995, pages 58-63, XP000517174 ISSN: 0018-9383 abstract; figure 1	1
A	LUNARDI L M ET AL: "Integrated p-i-n/HBT photoreceivers for optical communications" ELECTRON DEVICES MEETING, 1996., INTERNATIONAL SAN FRANCISCO, CA, USA 8-11 DEC. 1996, NEW YORK, NY, USA,IEEE, US, 8 December 1996 (1996-12-08), pages 645-648, XP010207625 ISBN: 0-7803-3393-4 abstract	
A	US 5 422 501 A (BAYRAKTAROGLU BURHAN) 6 June 1995 (1995-06-06) abstract	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 01/05527

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5422501 A	06-06-1995	US 5166083 A	24-11-1992
		EP 0505942 A1	30-09-1992
		JP 3249169 B2	21-01-2002
		JP 5090286 A	09-04-1993